

Fig. 1

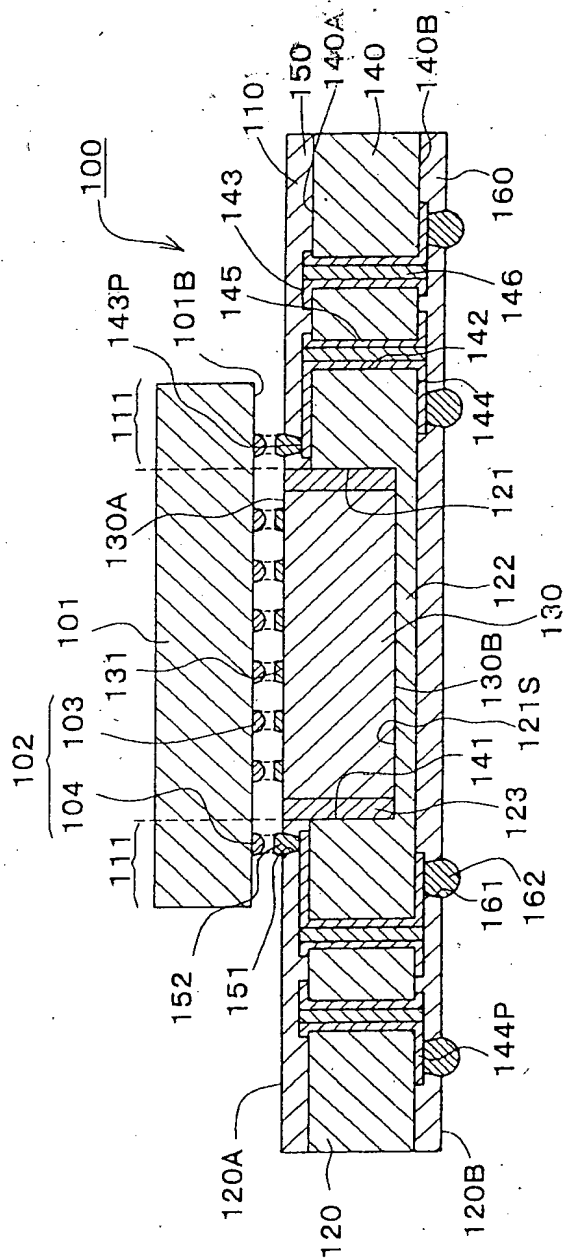


Fig. 2 (a)

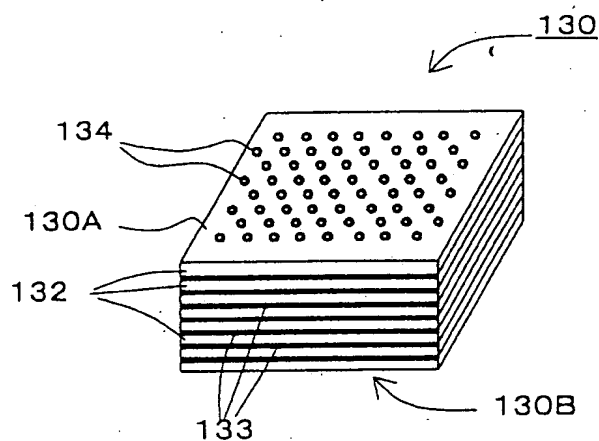


Fig. 2 (b)

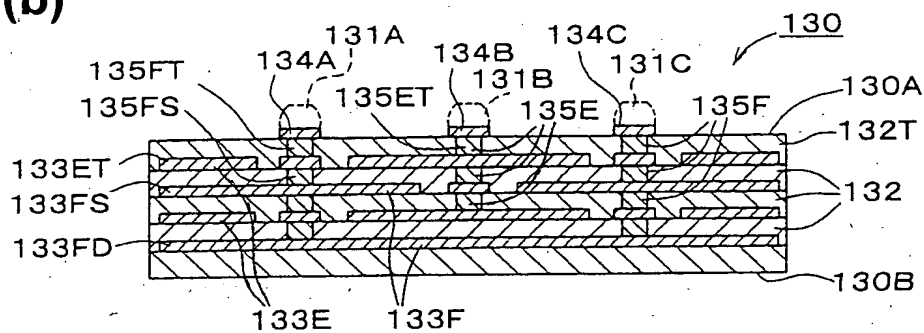


Fig. 2 (c)

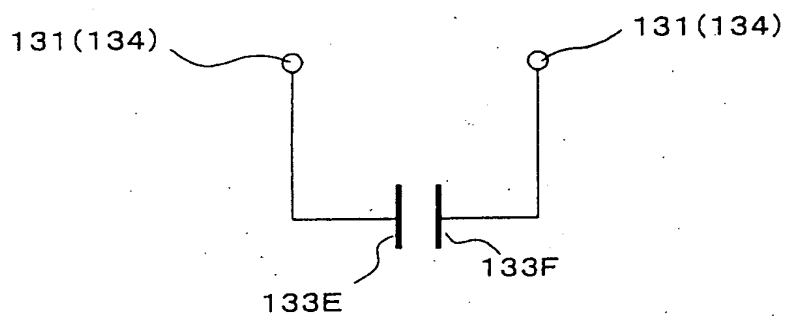


Fig. 3 (a)

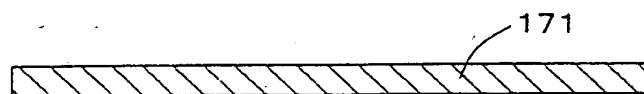


Fig. 3 (b)

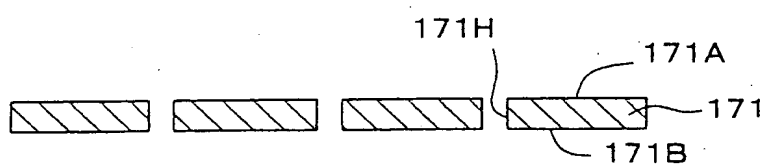
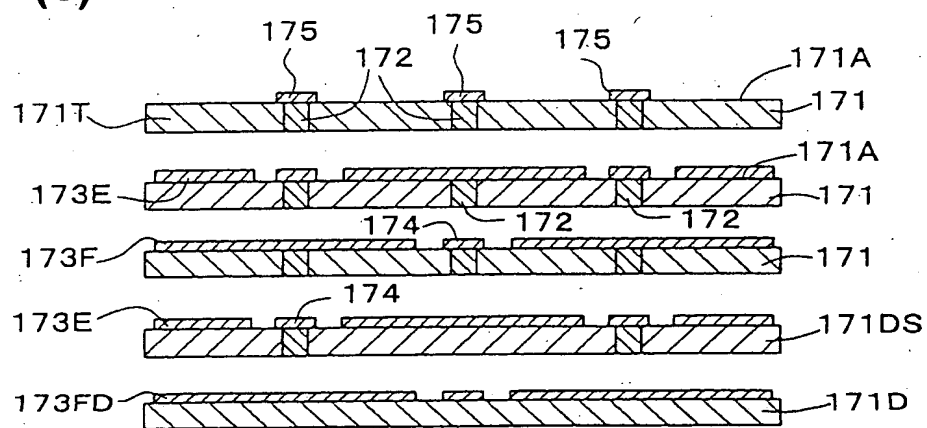


Fig. 3 (c)





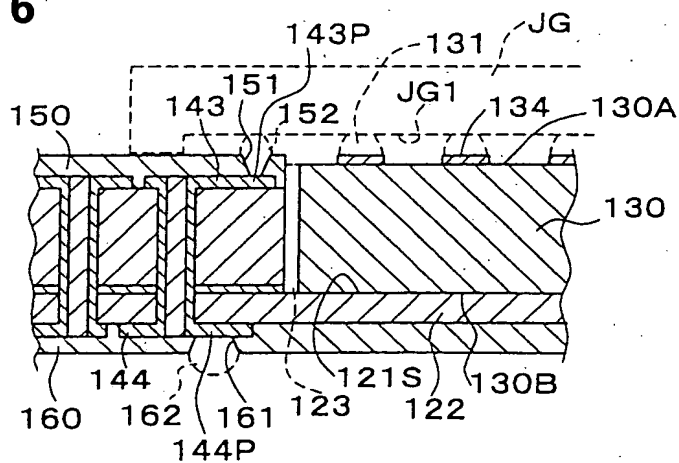
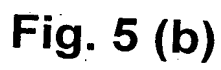
[illegible]

Fig. 7 (a)

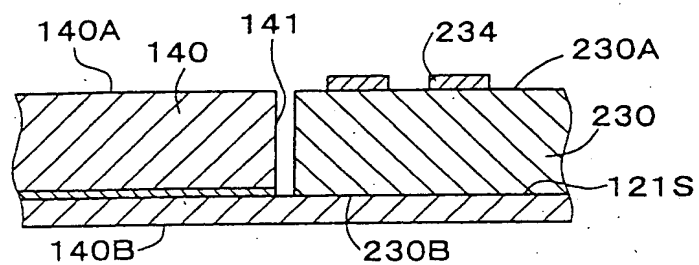


Fig. 7 (b)

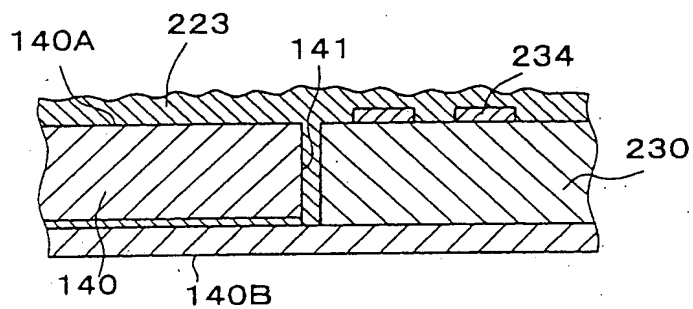
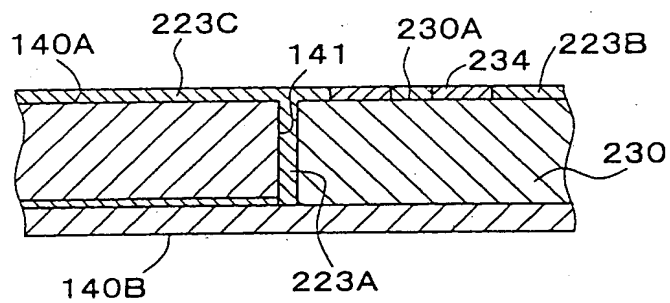


Fig. 7 (c)



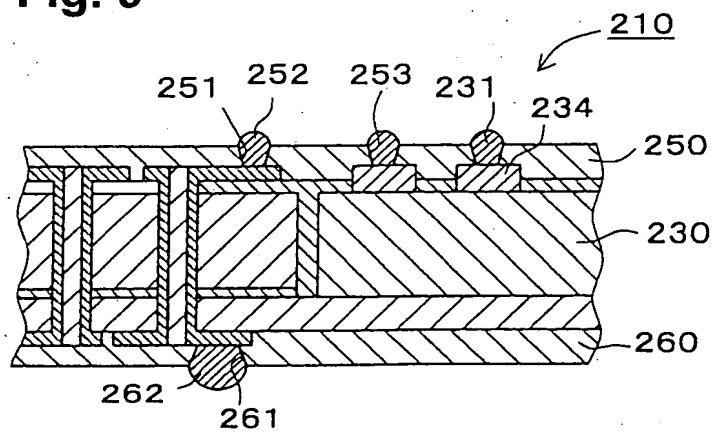
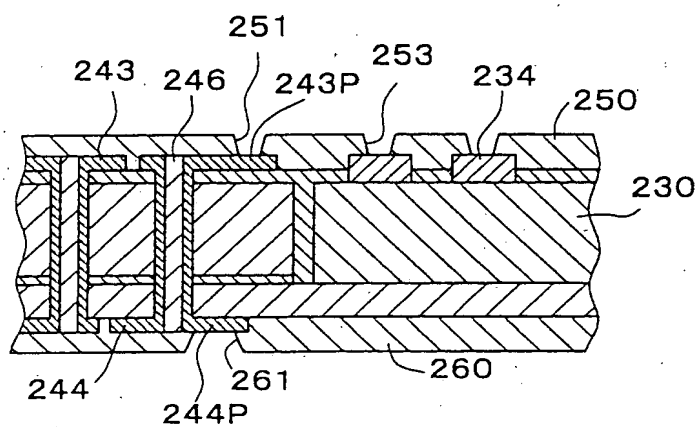
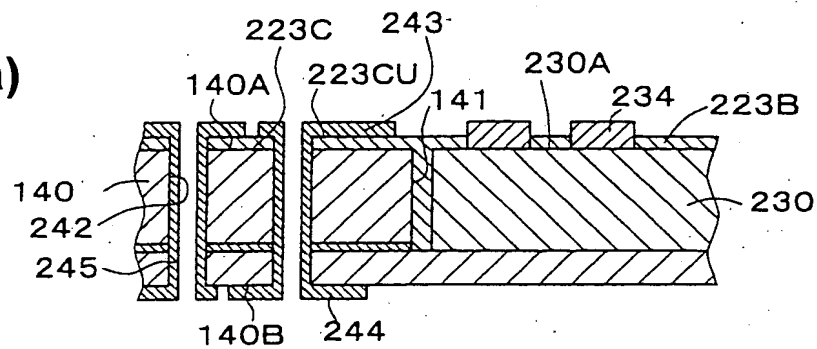


Fig. 10

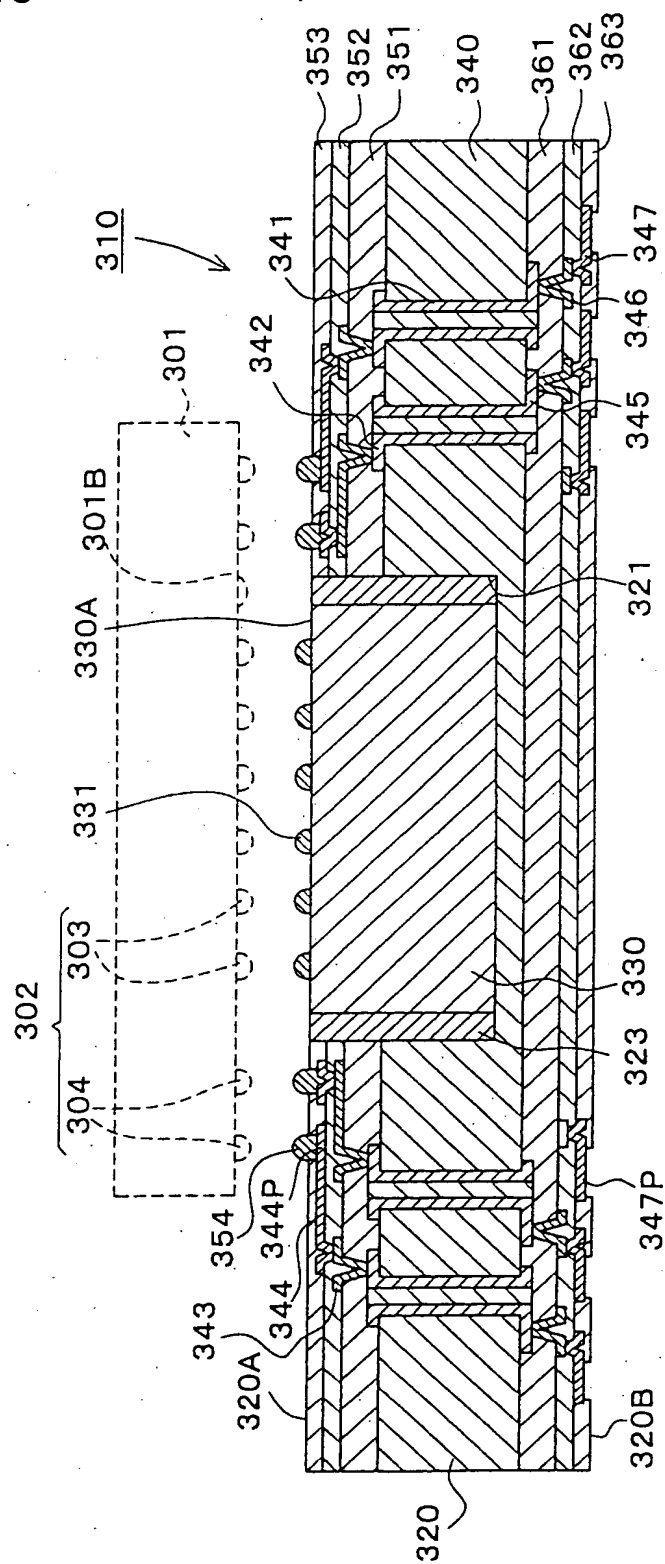




Fig. 11

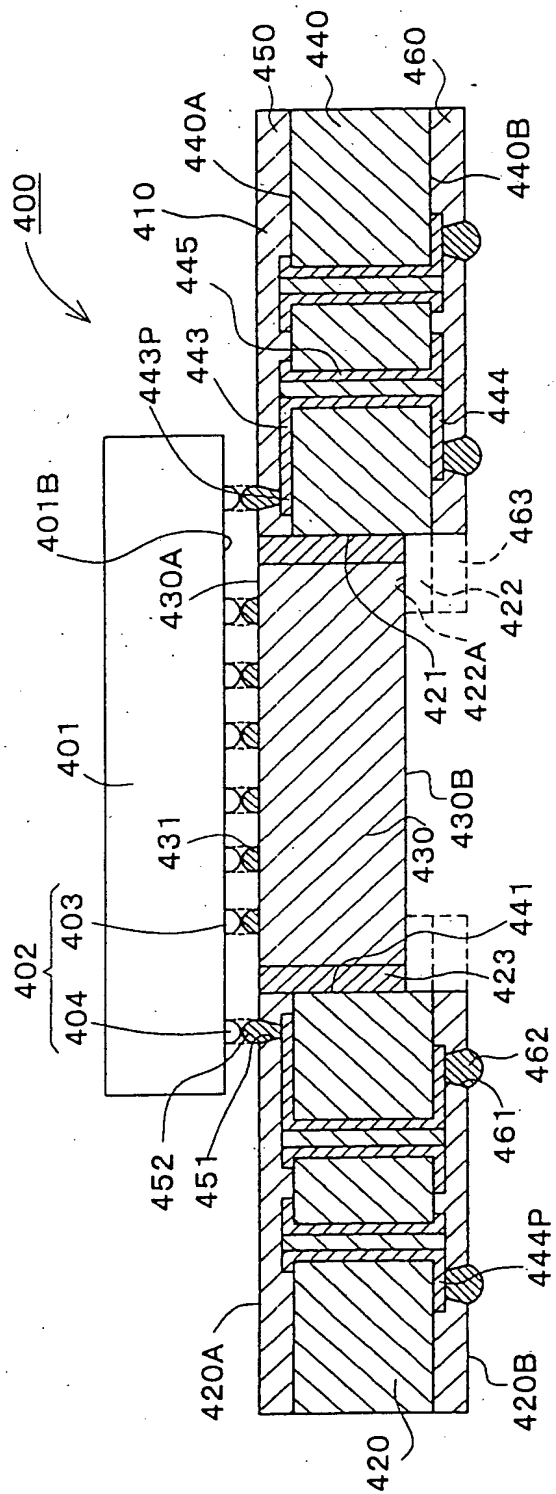






Fig. 14

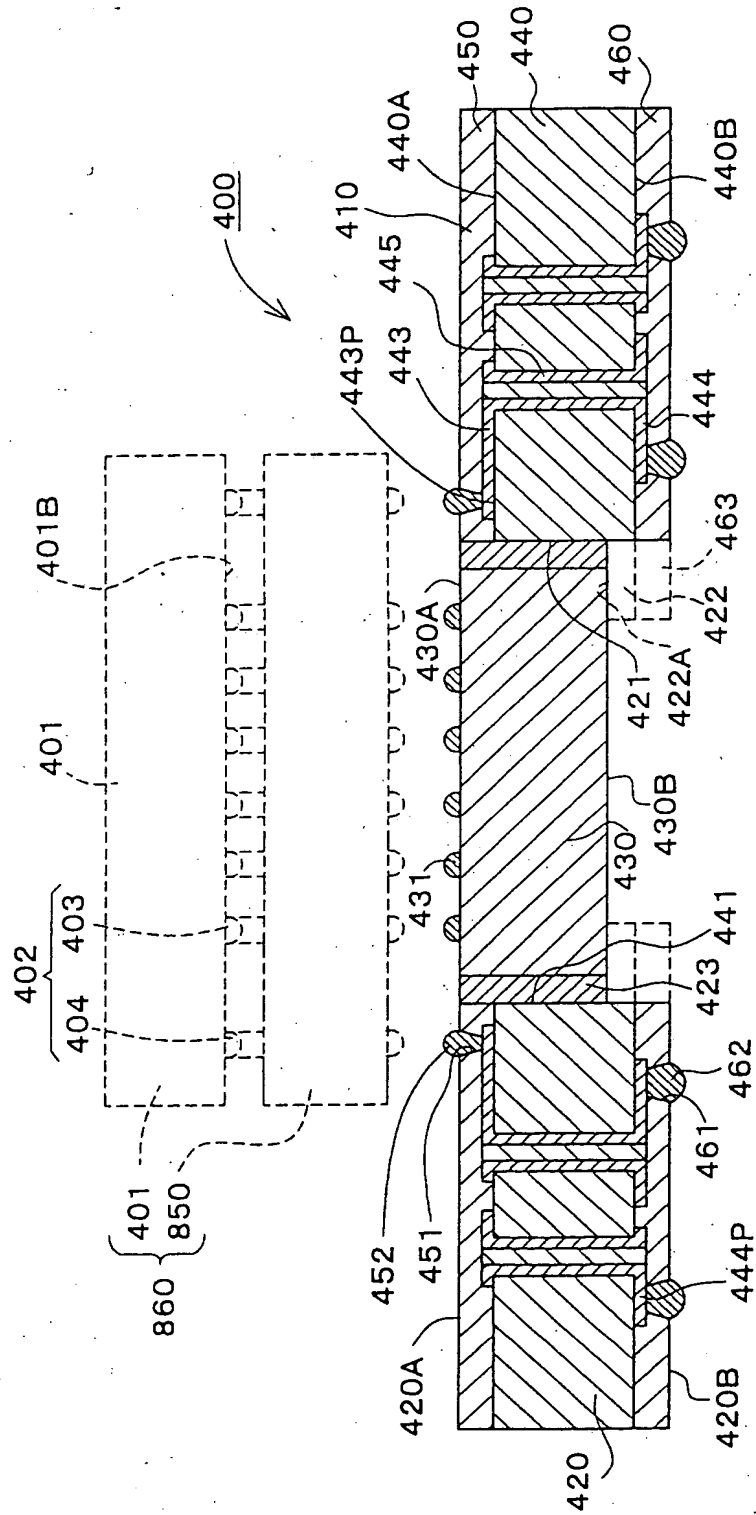




Fig. 16 (a)

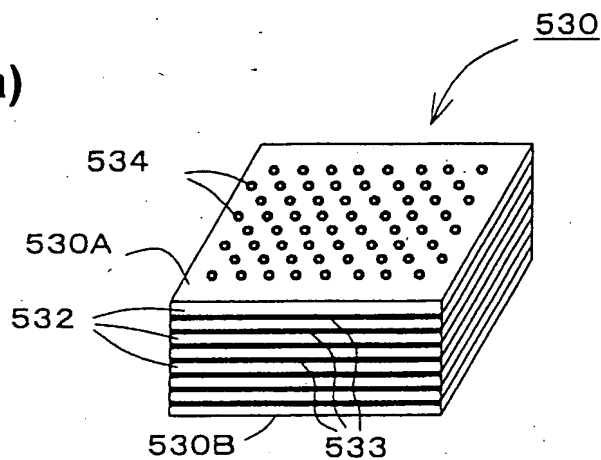


Fig. 16 (b)

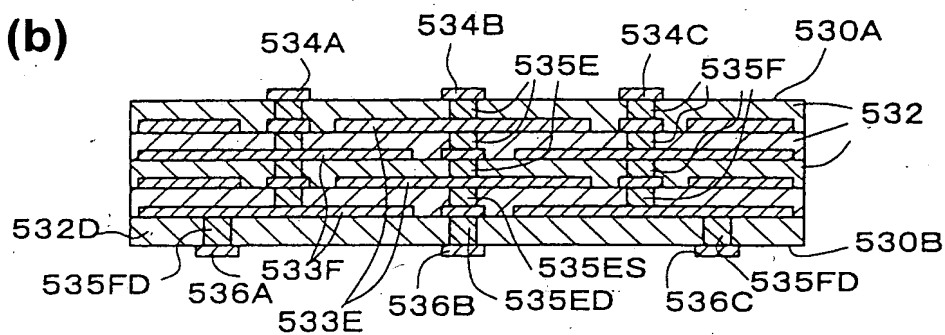
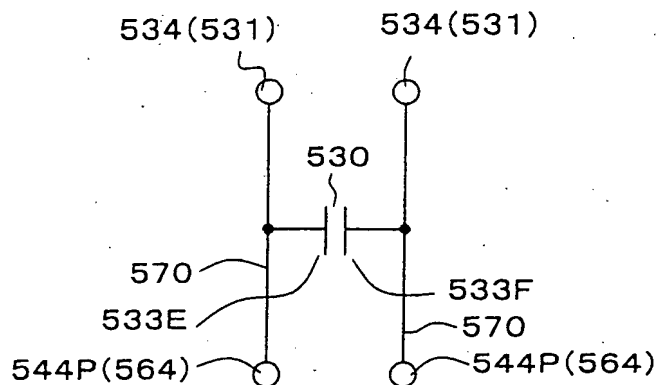
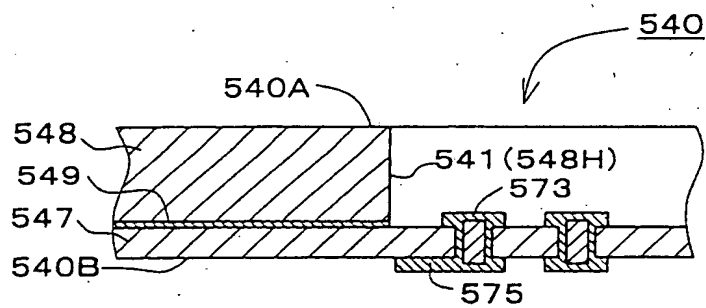
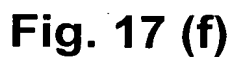
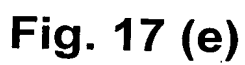
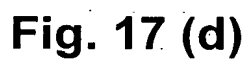
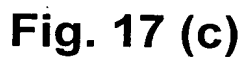


Fig. 16 (c)



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(a)

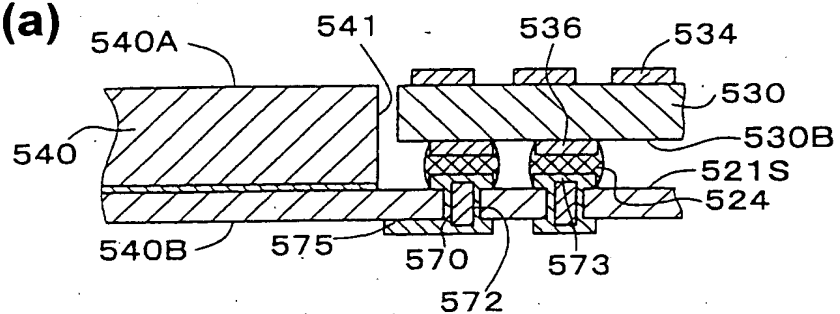
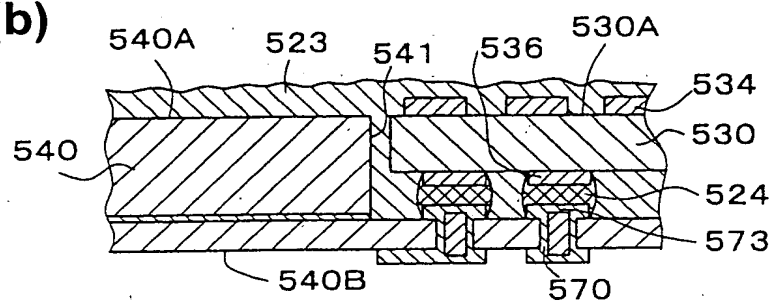
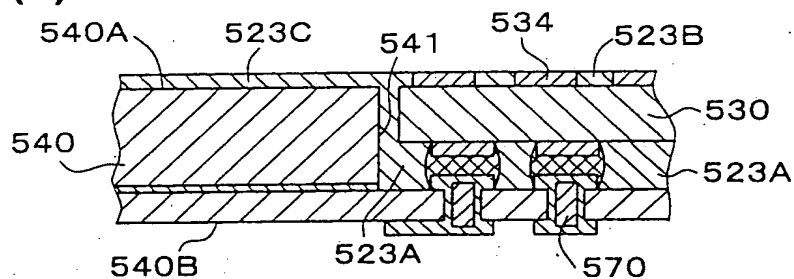
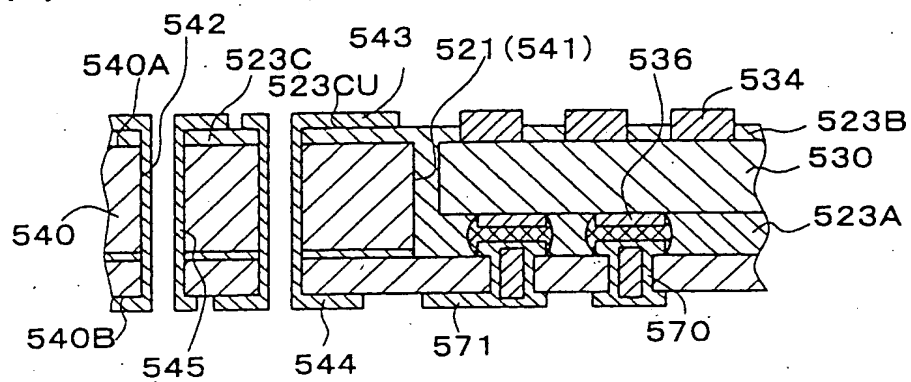


Fig. 1b is a cross-sectional view of a semiconductor device. It shows a substrate 540 with a top layer 540A and a bottom layer 540B. A central region 523 is defined by a vertical wall 541. On the right side, there is a structure 530 with a top layer 530A and a bottom layer 534. A layer 536 is located between the central region 523 and the structure 530. A layer 524 is located between the bottom layer 540B and the bottom layer 534. A layer 573 is located between the bottom layer 540B and the bottom layer 534. A layer 570 is located between the bottom layer 540B and the bottom layer 534.

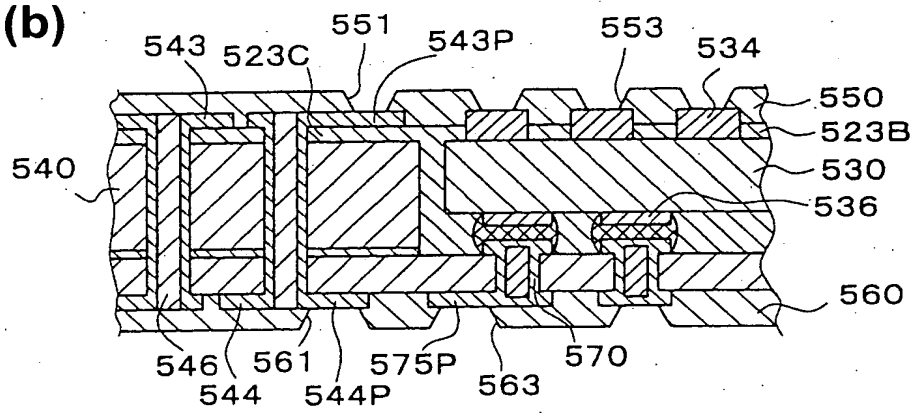
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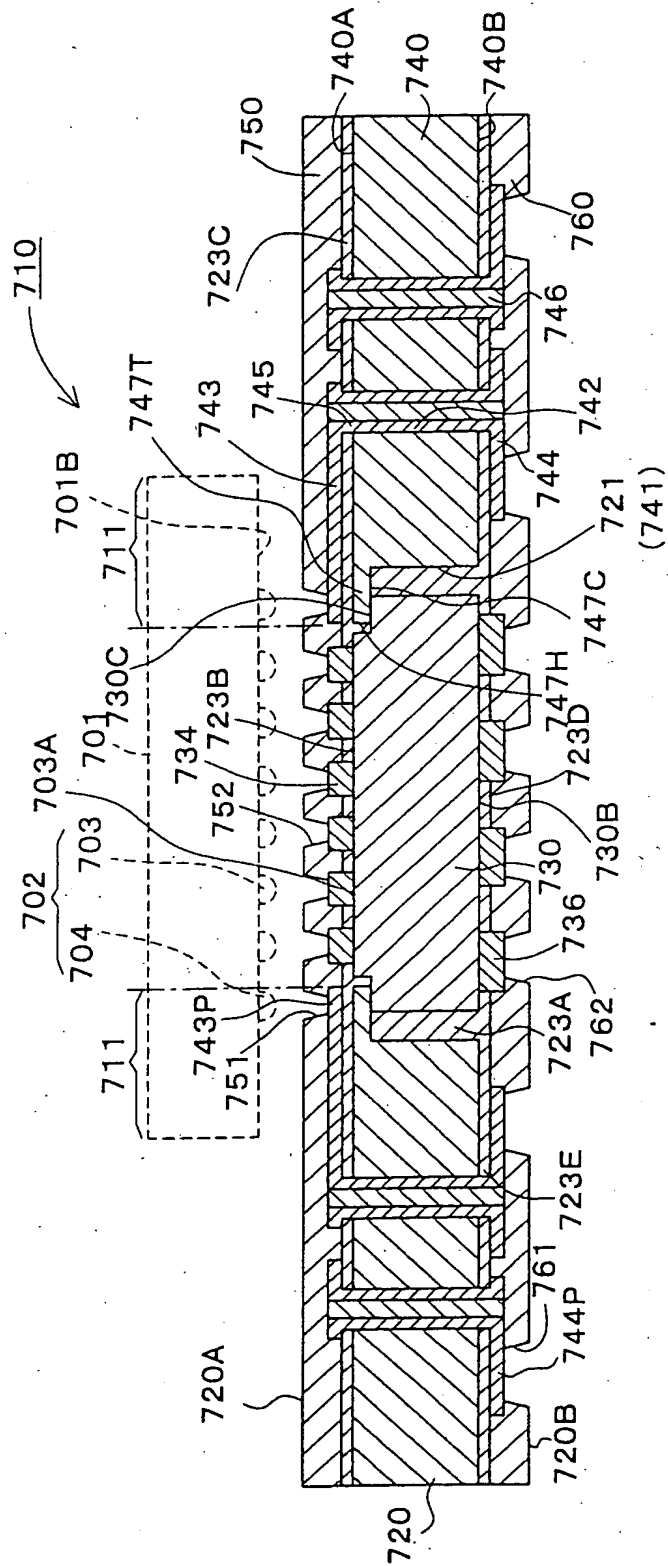
**Fig. 19 (a)**



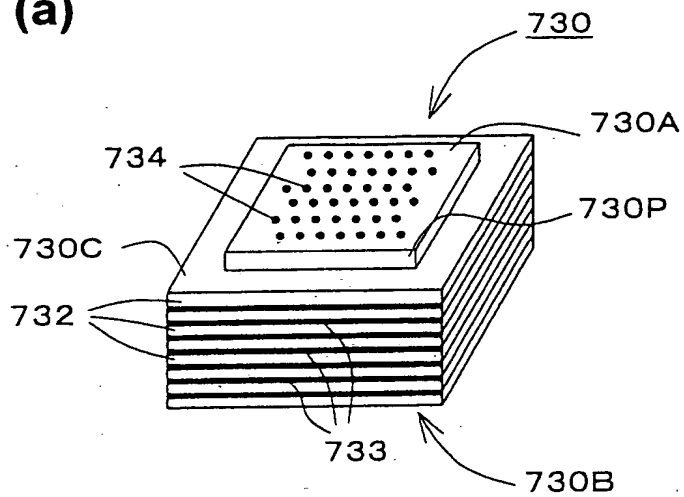
**Fig. 19 (b)**







**Fig. 22 (a)**



**Fig. 22 (b)**

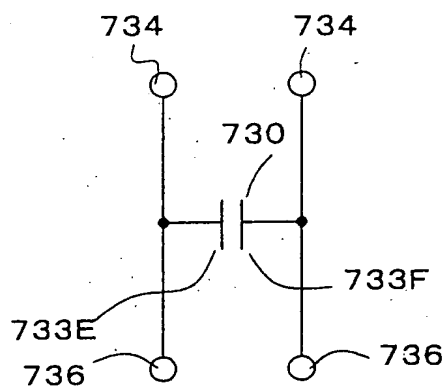


Fig. 23 (a)

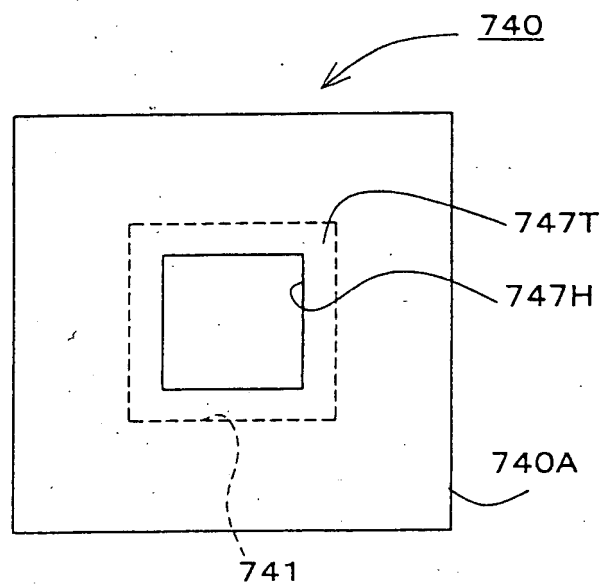
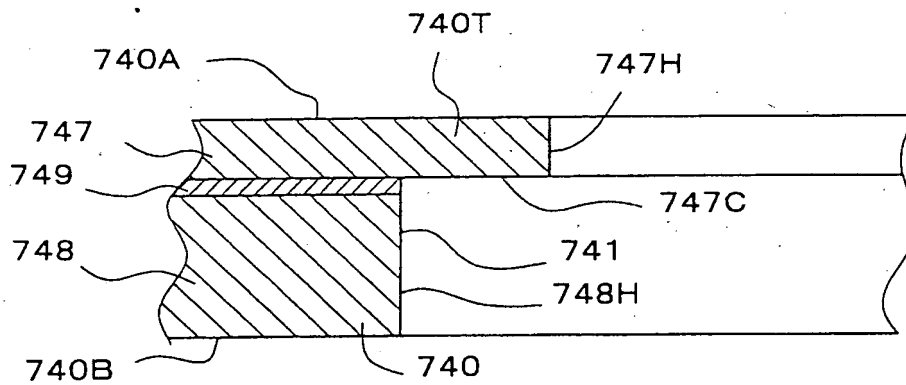
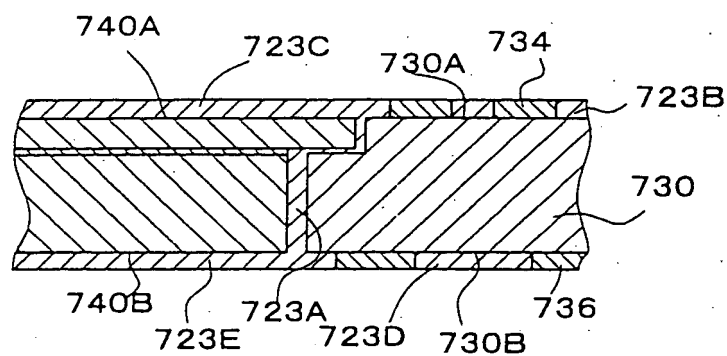
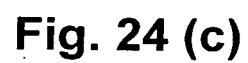
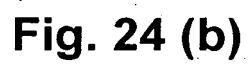
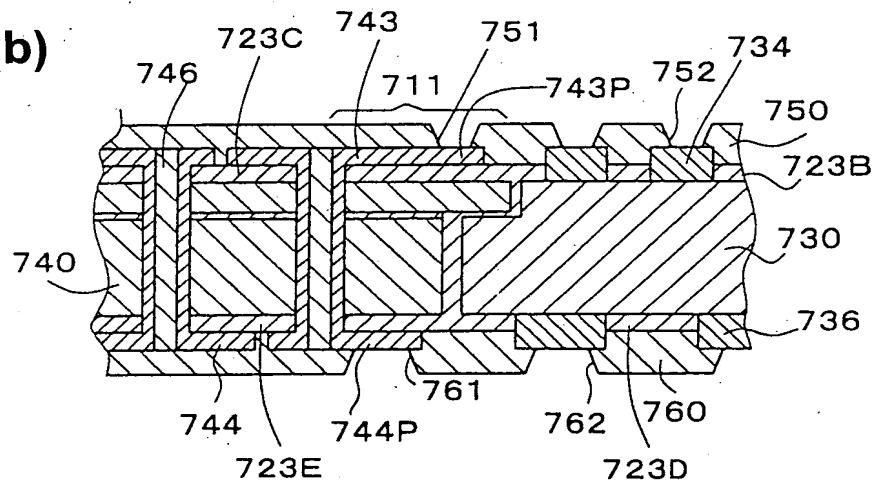
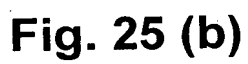


Fig. 23 (b)



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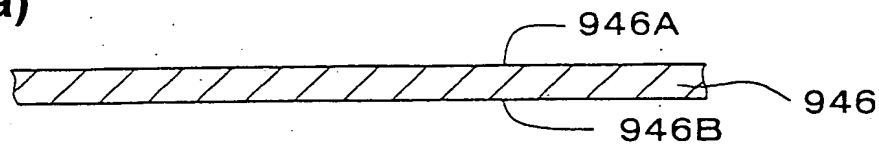


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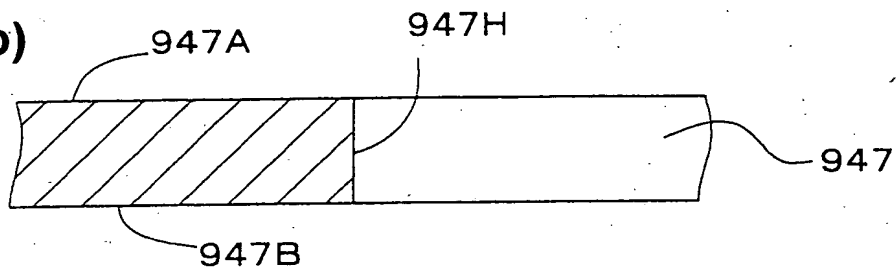
**Fig. 26**



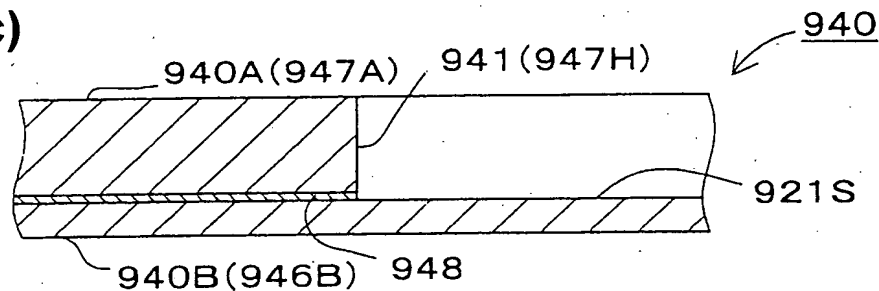
**Fig. 27 (a)**



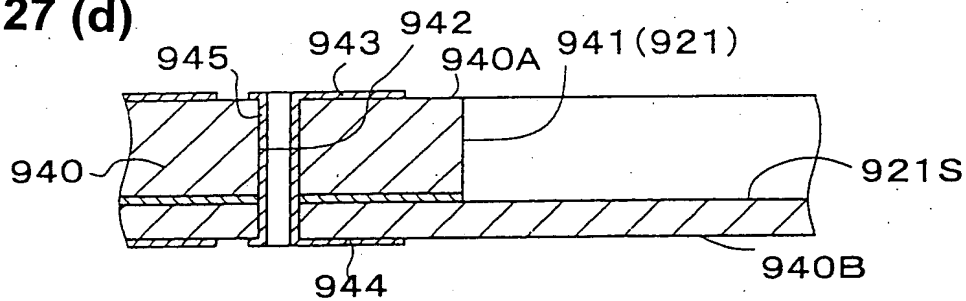
**Fig. 27 (b)**



**Fig. 27 (c)**



**Fig. 27 (d)**



**Fig. 27 (e)**

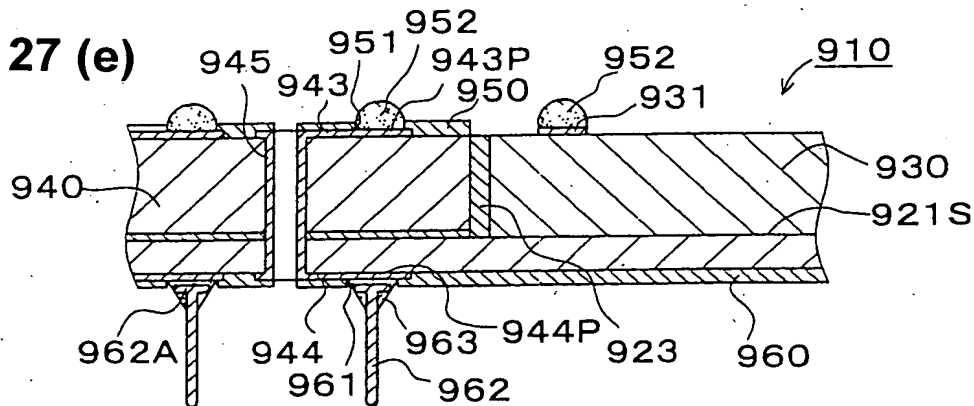


Fig. 28

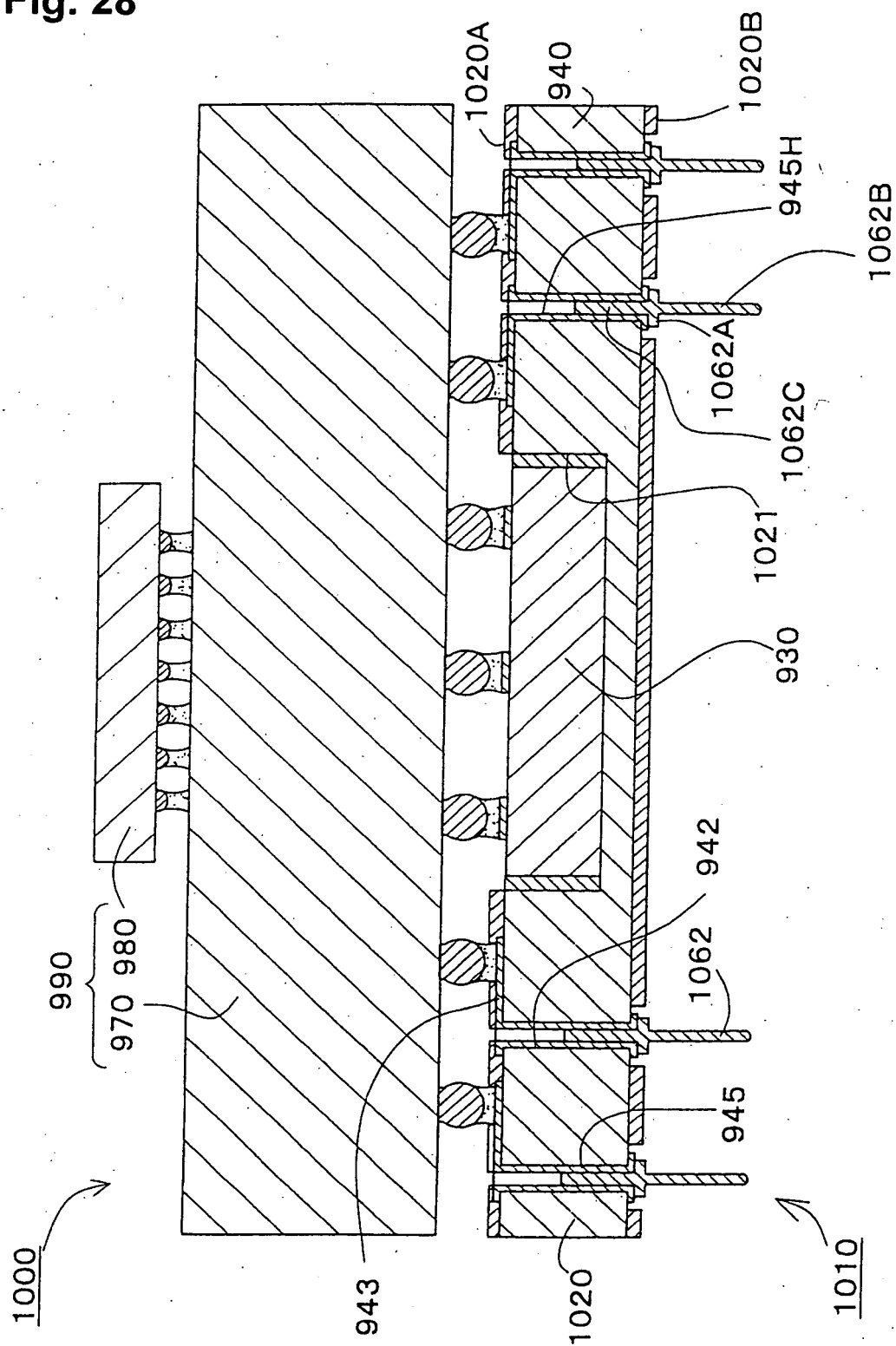
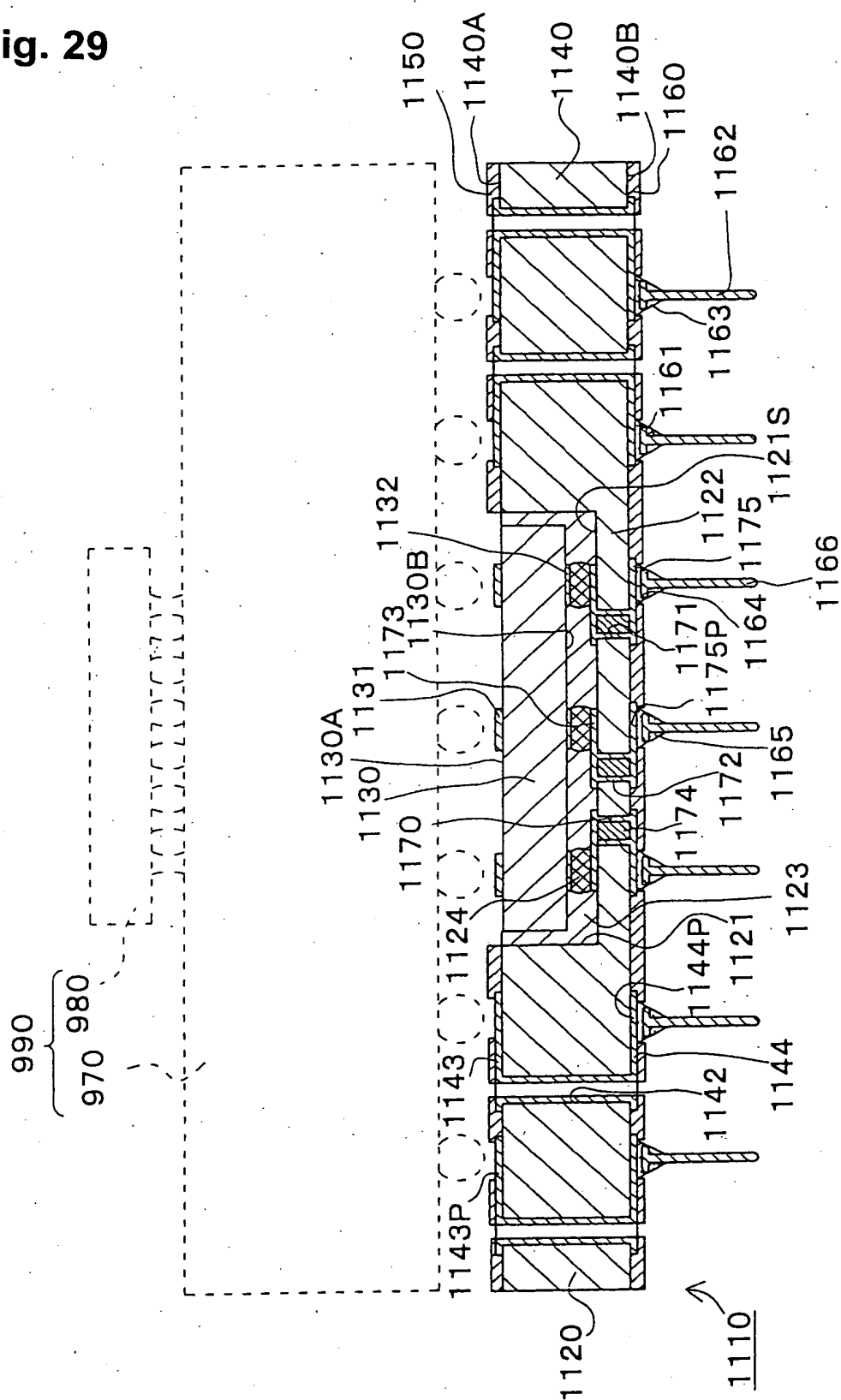


Fig. 29



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